

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 125 MHz
- 72 macrocells with 1,600 usable gates
- Up to 72 user I/O pins
- 5 V in-system programmable (ISP)
 - Endurance of 10,000 program/erase cycles
 - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
 - 90 product terms drive any or all of 18 macrocells within Function Block
 - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slow rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-7, -10 speed grades)
- Advanced 0.6 μ m CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 84-pin PLCC, 100-pin PQFP and 100-pin TQFP packages
- Plug-in compatible, non-ISP XC9572F available in 84-pin PLCC and 100-pin PQFP packages

Description

The XC9572 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of four 36V18 Function Blocks, providing 1,600 usable gates with propagation delays of 7.5 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC9572 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} \text{ (mA)} = MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 \text{ mA/MHz}) f$$

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

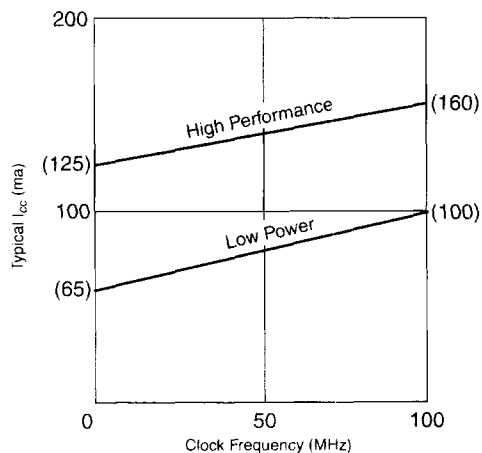
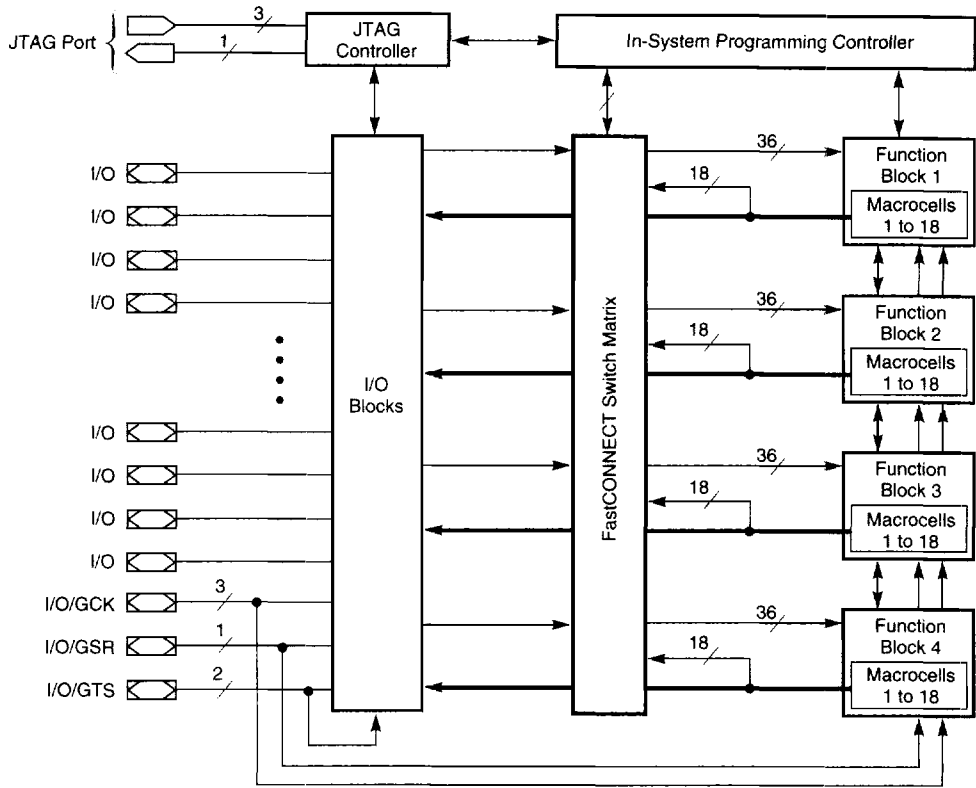


Figure 1: Typical I_{CC} vs. Frequency for XC9572



X5621

Figure 2: XC9572 Architecture

Note: Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 ns @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions¹

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	$V_{CCINT} + 0.5$	V
V_O	Output voltage	0	$V_{CCINT} + 0.5$	V

Note: 1. Numbers in parenthesis are for industrial temperature range versions.

Endurance Characteristics

Symbol	Parameter	Min	Max	Units
t_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles	10,000	-	Cycles

DC Characteristics Over Recommended Operating Conditions

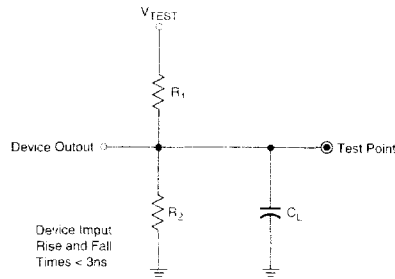
Symbol	Parameter	Test Conditions	Min	Max	Units
V _{OH}	Output high voltage for 5 V operation	I _{OH} = -4.0 mA V _{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I _{OH} = -3.2 mA V _{CC} = Min	2.4		V
V _{OL}	Output low voltage for 5 V operation	I _{OL} = 24 mA V _{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I _{OL} = 10 mA V _{CC} = Min		0.4	V
I _{IL}	Input leakage current	V _{CC} = Max V _{IN} = GND or V _{CC}		±10.0	μA
I _{IH}	I/O high-Z leakage current	V _{CC} = Max V _{IN} = GND or V _{CC}		±10.0	μA
C _{IN}	I/O capacitance	V _{IN} = GND f = 1.0 MHz		10.0	pF
I _{CC}	Operating Supply Current (low power mode, active)	V _I = GND, No load f = 1.0 MHz	65 (Typ)		ma

AC Characteristics

Symbol	Parameter	XC9572-7		XC9572-10		XC9572-15		Units
		Min	Max	Min	Max	Min	Max	
t _{PD}	I/O to output valid		7.5		10.0		15.0	ns
t _{SU}	I/O setup time before GCK	5.5		6.5		8.0		ns
t _H	I/O hold time after GCK	0.0		0.0		0.0		ns
t _{CO}	GCK to output valid		5.5		6.5		8.0	ns
f _{CNT} ¹	16-bit counter frequency	125		111		95		MHz
f _{SYSTEM} ²	Multiple FB internal operating frequency	83		67		56		MHz
t _{PSU}	I/O setup time before p-term clock input	1.5		2.5		4.0		ns
t _{PH}	I/O hold time after p-term clock input	4.0		4.0		4.0		ns
t _{PCO}	P-term clock to output valid		9.5		10.5		12.0	ns
t _{OE}	GTS to output valid		7.0		10.0		15.0	ns
t _{OD}	GTS to output disable		7.0		10.0		15.0	ns
t _{POE}	Product term OE to output enabled		13.0		15.5		18.0	ns
t _{POD}	Product term OE to output disabled		13.0		15.5		18.0	ns
t _{WLH}	GCK pulse width (High or Low)		4.0		4.5		5.5	ns

Preliminary

- Note:**
- f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable. f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
 - f_{SYSTEM} is the internal operating frequency for general purpose system designs spanning multiple FBs.



V _{CCIO} Level	V _{TEST}	R ₁	R ₂	C _L
5 V	5.0 V	160 Ω	120 Ω	35 pF
3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5222

Figure 3: AC Load Circuit

Internal Timing Parameters

Symbol	Parameter	XC9572-7		XC9572-10		XC9572-15		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
t _{IN}	Input buffer delay		2.5		3.5		4.5	ns
t _{GCK}	GCK buffer delay		2.5		3.0		3.0	ns
t _{GSR}	GSR buffer delay		4.5		6.0		7.5	ns
t _{GTS}	GTS buffer delay		7.0		10.0		15.0	ns
t _{OUT}	Output buffer delay		2.5		3.0		4.5	ns
t _{EN}	Output buffer enable/disable delay		0.0		0.0		0.0	ns
Product Term Control Delays								
t _{PTCK}	Product term clock delay		4.0		3.5		2.5	ns
t _{PTSR}	Product term set/reset delay		2.0		2.5		3.0	ns
t _{PTTS}	Product term 3-state delay		10.5		12.0		13.5	ns
Internal Register and Combinatorial delays								
t _{PDI}	Combinatorial logic propagation delay		0.5		1.0		3.0	ns
t _{SUI}	Register setup time	3.5		3.5		3.5		ns
t _{HI}	Register hold time	2.0		3.0		4.5		ns
t _{COI}	Register clock to output valid time		0.5		0.5		0.5	ns
t _{AOI}	Register async. S/R to output delay		6.5		7.0		8.0	ns
t _{RAI}	Register async. S/R recovery before clock	7.5		10.0		15.0		ns
t _{LOGI}	Internal logic delay		2.0		2.5		3.0	ns
t _{LOGILP}	Internal low power logic delay		10.0		11.0		11.5	ns
Feedback Delays								
t _F	FastCONNECT matrix feedback delay		6.0		8.5		11.0	ns
t _{LF}	Function Block local feedback delay		2.0		2.5		3.5	ns
Time Adders								
t _{PTA} ³	Incremental Product Term Allocator delay		1.0		1.0		1.5	ns
t _{SLEW}	Slew-rate limited delay		4.0		4.5		5.0	ns
Preliminary								

Note: 3. t_{PTA} is multiplied by the span of the function as defined in the family data sheet.

XC9572 I/O Pins

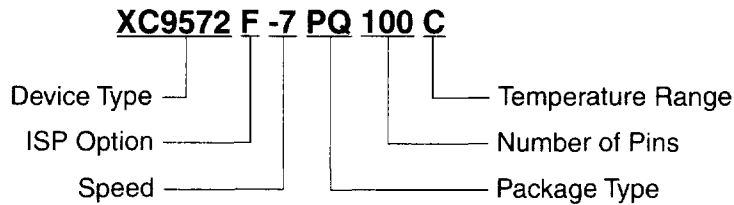
Function Block	Macrocell	PC84	PQ100	TQ100	BScan Order	Notes	Function Block	Macrocell	PC84	PQ100	TQ100	BScan Order	Notes
1	1	4	18	16	213		3	1	25	43	41	105	
1	2	1	15	13	210		3	2	17	34	32	102	
1	3	6	20	18	207		3	3	31	51	49	99	
1	4	7	22	20	204		3	4	32	52	50	96	
1	5	2	16	14	201		3	5	19	37	35	93	
1	6	3	17	15	198		3	6	34	55	53	90	
1	7	11	27	25	195		3	7	35	56	54	87	
1	8	5	19	17	192		3	8	21	39	37	84	
1	9	9	24	22	189	[1]	3	9	26	44	42	81	
1	10	13	30	28	186		3	10	40	62	60	78	
1	11	10	25	23	183	[1]	3	11	33	54	52	75	
1	12	18	35	33	180		3	12	41	63	61	72	
1	13	20	38	36	177		3	13	43	65	63	69	
1	14	12	29	27	174	[1]	3	14	36	57	55	66	
1	15	14	31	29	171		3	15	37	58	56	63	
1	16	23	41	39	168		3	16	45	67	65	60	
1	17	15	32	30	165		3	17	39	60	58	57	
1	18	24	42	40	162		3	18	—	61	59	54	
2	1	63	89	87	159		4	1	46	68	66	51	
2	2	69	96	94	156		4	2	44	66	64	48	
2	3	67	93	91	153		4	3	51	73	71	45	
2	4	68	95	93	150		4	4	52	74	72	42	
2	5	70	97	95	147		4	5	47	69	67	39	
2	6	71	98	96	144		4	6	54	78	76	36	
2	7	76	5	3	141	[1]	4	7	55	79	77	33	
2	8	72	99	97	138		4	8	48	70	68	30	
2	9	74	1	99	135	[1]	4	9	50	72	70	27	
2	10	75	3	1	132		4	10	57	83	81	24	
2	11	77	6	4	129	[1]	4	11	53	76	74	21	
2	12	79	8	6	126		4	12	58	84	82	18	
2	13	80	10	8	123		4	13	61	87	85	15	
2	14	81	11	9	120		4	14	56	80	78	12	
2	15	83	13	11	117		4	15	65	91	89	9	
2	16	82	12	10	114		4	16	62	88	86	6	
2	17	84	14	12	111		4	17	66	92	90	3	
2	18	—	94	92	108		4	18	—	81	79	0	

Notes: [1] Global control pin

XC9572 Global, JTAG and Power Pins

Pin Type	PC84	PQ100	TQ100
I/O/GCK1	9	24	22
I/O/GCK2	10	25	23
I/O/GCK3	12	29	27
I/O/GTS1	76	5	3
I/O/GTS2	77	6	4
I/O/GSR	74	1	99
TCK	30	50	48
TDI	28	47	45
TDO	59	85	83
TMS	29	49	47
V _{CCINT} 5 V	38,73,78	7,59,100	5,57,98
V _{CCIO} 3.3 V/5 V	22,64	28,40,53,90	26,38,51,88
GND	8,16,27,42,49,60	2,23,33,46,64,71,77,86	100,21,31,44,62,69,75,84
No Connects	—	4,9,21,26,36,45,48,75,82	2,7,19,24,34,43,46,73,80

Ordering Information



ISP Options

- With ISP (blank)
- F Without ISP

Speed Options

- 15 15 ns pin-to-pin delay
- 10 10 ns pin-to-pin delay
- 7 7.5 ns pin-to-pin delay

Packaging Options

- PC84 84-Pin Plastic Leaded Chip Carrier (PLCC)
- PQ100 100-Pin Plastic Quad Flat Pack (PQFP)
- TQ100 100-Pin Very Thin Quad Flat Pack (TQFP)

Temperature Options

- C Commercial 0°C to 70°C
- I Industrial -40°C to 85°C

Component Availability

Pins		84		100	
		Plastic PLCC	Plastic PQFP	Plastic PQFP	Plastic TQFP
Code		PC84	PQ100	TQ100	
XC9572	-15	C(I)	C(I)	C(I)	
	-10	C(I)	C(I)	C(I)	
	-7	C	C	C	
XC9572F	-15	C(I)	C(I)	-	
	-10	C(I)	C(I)	-	
	-7	C	C	-	

C = Commercial = 0° to +70°C I = Industrial = -40° to 85°C